IN THE SPECIFICATION

Please replace the paragraph beginning at page 11, line 1, with the following:

The formation of contact plugs 320 and ~~340~~ 340'and storage node contact plugs 340 on the contact pads 240 and 250 according to a general DRAM process will be described with reference to FIGS. 9 and 10.

Please replace the paragraph beginning at page At page 12, lines 7 with the following:

Referring to FIG. 10, capacitors 350 each including a capacitor lower electrode 352, a capacitor dielectric layer 354, and a capacitor upper electrode 356, metal contact plugs ~~340~~ 340', and metal interconnections 360 are formed on the semiconductor substrate that has undergone the above steps. As a result, the basic structure of a DRAM having transistors C_N, P_N, P_P and capacitors 350 is formed. Here, the formation of the capacitors 350, the metal contact plugs ~~340~~ 340', and the metal interconnections 360 are known in the art and thus the detailed description of the steps is omitted.

Please replace the paragraph beginning at page at page 12, line 25, with the folowwing:

Advantages obtained by using metal contact pads are as follows. In general, highly doped polysilicon has sheet resistance of about 200 ~ 400 Ω/Q. This is much greater than sheet resistance of a metal such as tungsten. Consequently, ~~the?~~ the contact resistance between contact pads and source/drain regions interferes with the integration of semiconductor devices. For this reason, metal contact pads are preferred to prevent the reduction of current driving power due to parasitic resistance of source/drain regions. In detail, in the plane of the semiconductor substrate shown in FIG. 16, when electric current flows from a source 610 to a drain 620, distance to contact pads 640 vary depending on paths P_1 and P_2 taken by the electric current, shown by a dotted line, through a gate electrode 630. As a result, voltage drops, and current driving power is reduced. To reduce parasitic resistance, the contact pads 640 are required to be formed on several places in the source 610 and drain 620. Thus, the active area widens, which is disadvantageous for the size of chips. In case of metal contact pads, voltage drops slightly due to resistance dependent on the current flowing distance. Thus, one contact pad 640 may be formed on a source 610 and a drain 620.